What is claimed is:

1. A method of driving a liquid crystal display, comprising the steps of:

receiving a data enable signal for indicating a time interval when a video data exists;

detecting an enable initiation time of the data enable signal;

generating a reset signal at said enable initiation time of the data enable signal; and

resetting a source shift clock for sampling the video data in response to the reset signal.

2. The method according to claim 1, further comprising the steps of:

sampling and then latching the video data in response to the source shift clock;

applying the latched video data to data lines of a liquid crystal display panel; and

sequentially applying scanning pulses to gate lines of the liquid crystal display panel.

3. A driving apparatus for a liquid crystal display, comprising:

a reset signal generator for detecting an enable initiation time of a data enable signal for indicating a time interval when a vide data exists to generate a reset signal; and

reset means for resetting a source shift clock for sampling the video data at said enable initiation time.

4. The driving apparatus according to claim 3, further comprising:

a liquid crystal display panel having liquid crystal cells provided at pixel areas between the data lines and the gate lines perpendicularly crossing each other and thin film transistors provided at intersections between the data lines and the gate lines to drive the liquid crystal cells;

a source driver for sampling and then latching the video data in response to the source shift clock and for applying the latched data to the data lines of the liquid crystal display panel; and

a gate driver for sequentially applying scanning pulses to the gate lines of the liquid crystal display panel to select scanning lines; and

a timing controller for controlling the source driver and the gate driver.

5. The driving apparatus according to claim 4, wherein the reset signal generator and the reset means are included in the timing controller.

6. The driving apparatus according to claim 3, wherein the reset signal generator includes:

a D flip-flop for receiving the data enable signal and a dot clock via an input line to delay the data enable signal in accordance with the dot clock; and

an inverter for inverting the delayed data enable signal;

an AND gate for making a logical product operation of the delayed and inverted enable signal and the data enable signal from the input line to generate a reset signal for indicating an enable initiation time of the data enable signal.

7. The driving apparatus according to claim 6, wherein the reset means toggles the dot clock to generate the source shift clock and resets the source shift clock in response to the reset signal.